CLASS D AMPLIFIER DRIVER

V900

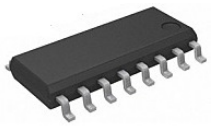
1. GENERAL DESCRIPTION

The V900 is a high voltage, high speed MOSFET driver with a floating PWM input designed for Class D audio amplifier applications. Bi-directional current sensing detects over-current conditions during positive and negative load currents without any external shunt resistors. A built-in protection control block provides a secure protection sequence against over current conditions and a programmable reset timer. The internal dead time generation block enables accurate gate switching and optimum dead time setting for better audio performance, such as lower THD and lower audio noise floor.

FEATURES

- Programmable constant current mode OCP timer.
- Programmable preset dead-time for improved
- THD performances.
- Programmable bidirectional over-current
- protection with self-reset function.
- High noise immunity.
- +/-100 V ratings deliver up to 500 W in output power.
- 3.3V/5 V logic compatible input.
- Operates up to 800 kHz.
- RoHS compliant.

2. PIN CONFIGURATION



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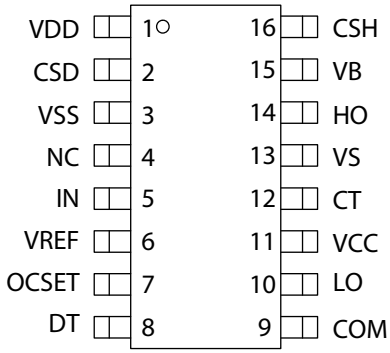

3. TYPICAL APPLICATIONS

- Class D amplifier driver

4. PIN DESCRIPTION

No.	Name	Functions Description	No.	Name	Functions Description
1	VDD	Floating positive supply	9	COM	Low side supply return
2	CSD	Shutdown timing capacitor, referenced to VSS	10	LO	Low side output
3	VSS	Floating supply return	11	VCC	Low side logic supply
4	NC	No Connect	12	CT	OCP timing capacitor, referenced to VCC
5	IN	PWM non-inverting input referenced to COM, in phase with HO	13	VS	High side floating supply return
6	VREF	5V reference output for setting OCSET	14	HO	High side output
7	OCSET	Low side over current threshold setting, referenced to COM	15	VB	High side floating supply
8	DT	Input for programmable deadtime, referenced to COM	16	CSH	High side over current sensing input, referenced to VS

5. FUNCTIONAL BLOCK DIAGRAM

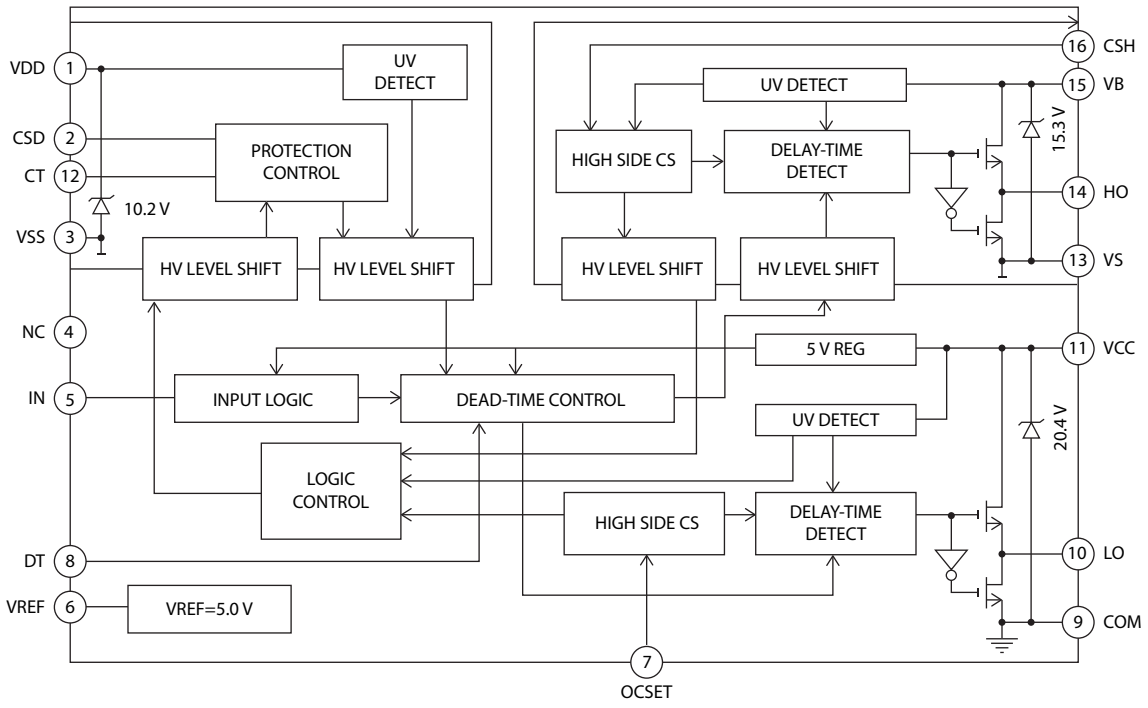

Figure 1. Functional Block Diagram

6. ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min.	Typ.	Max.
V_B	High side floating supply voltage	-0.3	215	V
V_S	High side floating supply voltage (Note1)	V_B -15	V_B +0.3	
V_{HO}	High side floating output voltage	V_S -0.3	V_B +0.3	
V_{CSH}	CSH pin input voltage	V_S -0.3	V_B +0.3	
V_{CC}	Low side fixed supply voltage (Note1)	-0.3	20	
V_{LO}	Low side output voltage	-0.3	V_{CC} +0.3	
V_{DD}	Floating input supply voltage	-0.3	210	
V_{SS}	Floating input supply voltage (Note1)	(See I_{DDZ})	V_{DD} +0.3	
V_{IN}	PWM input voltage	-0.3	V_{CC} +0.3	
V_{CT}	CT pin input voltage	-0.3	V_{CC} +0.3	
V_{CSD}	CSD pin input voltage	V_{SS} -0.3	V_{DD} +0.3	
V_{DT}	DT pin input voltage	-0.3	V_{CC} +0.3	
V_{OCSET}	OCSET pin input voltage	-0.3	V_{CC} +0.3	
V_{REF}	VREF pin voltage	-0.3	V_{CC} +0.3	
I_{DDZ}	Floating input supply zener clamp current (Note1)	—	10	mA
I_{CCZ}	Low side supply zener clamp current (Note1)	—	10	
I_{BSZ}	Floating supply zener clamp current (Note1)	—	10	
I_{OREF}	Reference output current	—	5	
dV_S/dt	Allowable VS voltage slew rate	—	50	V/ns
dV_{SS}/dt	Allowable VSS voltage slew rate (Note2)	—	50	
dV_{SS}/dt	Allowable VSS voltage slew rate upon power-up	—	50	V/ms
P_D	Maximum power dissipation	—	1.0	W
$R_{th,JA}$	Thermal resistance, Junction to ambient	—	115	°C/W
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead temperature (Soldering, 10 seconds)	—	300	

Note 1: V_{DD} - V_{SS}, V_{CC} - COM and V_B - V_S contain internal shunt zener diodes. Please note that the voltage ratings of these can be limited by the clamping current.

Note2: For the rising and falling edges of step signal of 10 V. V_{SS} = 15 V to 200 V.

7. RECOMMENDED OPERATING CONDITIONS

The device should be used within the recommended conditions below for proper operation. The V_S and COM offset ratings are tested with supplies biased at I_{DD} = 5 mA, V_{CC} = 12V and V_B -V_S = 12V.

Symbol	Parameter	Min.	Max.	Unit
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 18	V
V_S	High side floating supply offset voltage	(Note1)	100	
I_{DDZ}	Floating input supply zener clamp current	1	5	mA
V_{SS}	Floating input supply absolute voltage	0	200	V
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side fixed supply voltage	10	18	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	PWM input voltage	0	V_{CC}	
V_{CSD}	CSD pin input voltage	V_{SS}	V_{DD}	
V_{CT}	CT pin input voltage	0	V_{CC}	
V_{DT}	DT pin input voltage	0	V_{CC}	
I_{OREF}	Reference output current to COM (Note2)	0.3	0.8	mA
V_{OCSET}	OCSET pin input voltage	0.5	5	V
T_A	Ambient Temperature	-40	125	°C

Note1: Logic operational for V_S equal to -5 V to +200 V. Logic state held for V_S equal to-5 V to -V_{BS}.

Note1: Nominal voltage for V_{REF} is 5 V. I_{OREF} of 0.3 mA–0.8 mA dictates total external resistor value on V_{REF} to be 6.3 kΩ to 16.7 k.Ω

8. ELECTRICAL CHARACTERISTICS

(V_{CC}, V_{BS}=12 V, I_{DD}=5 mA, V_{SS}=20 V, V_S=0 V, C_L=1nF and T_A=25 °C unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
Low Side Supply						
UV_{CC+}	V_{CC} supply UVLO positive threshold	8.4	8.9	9.4	V	
UV_{CC-}	V_{CC} supply UVLO negative threshold	8.2	8.7	9.2		
I_{QCC}	Low side quiescent current	—	—	3	mA	V_{DT} = V_{CC}
V_{CLAMPL}	Low side zener diode clamp voltage	18.0	20.4	22.0	V	I_{CC} = 5 mA
High Side Floating Supply						
UV_{BS+}	High side well UVLO positive threshold	8	8.5	9	V	
UV_{BS-}	High side well UVLO negative threshold	7.8	8.3	8.8		
I_{QBS}	High side quiescent current	—	—	1	mA	
I_{LKH}	High to Low side leakage current	—	—	50	uA	V_B = V_S = 200 V
V_{CLAMPH}	High side zener diode clamp voltage	14.7	15.3	16.2	V	I_{BS} = 5 mA

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
Floating Supply						
UV_{DD+}	VDD, VSS floating supply UVLO positive threshold	8.2	8.7	9.2	V	V_{SS} = 0 V
UV_{DD-}	VDD, VSS floating supply UVLO negative threshold	7.7	8.2	8.7		V_{SS} = 0V
I_{QDD}	Floating Input quiescent current	—	—	1	mA	V_{DD} = 9.5V+V_{SS}
V_{CLAMPM}	Floating Input zener diode clamp voltage	9.8	10.2	10.8	V	I_{DD} = 5 mA
I_{LKM}	Floating input side to Low side leakage current	—	—	50	uA	V_{DD} = V_{SS} = 200 V
PWM Input						
V_{IH}	Logic high input threshold voltage	3.0	2.3	—	V	
V_{IL}	Logic low input threshold voltage	—	2.3	1.5		
I_{IN+}	Logic "1" input bias current	—	—	40	µA	V_{IN} = 3.3 V
I_{IN-}	Logic "0" input bias current	—	—	1		V_{IN} = 0
Protection						
V_{REF}	Reference output voltage	4.75	4.95	5.15	V	I_{OREF} = 0.5 mA
V_{thOCL}	Low side OC threshold in V_S	1.0	1.2	1.4		O_{CSET} = 1.2 V
V_{thOCH}	High side OC threshold in V_{CSH}	1.05+VS	1.2+VS	1.35+VS		V_S = 200 V
$V_{th,1}$	CSD pin shutdown release threshold	0.62xVDD	0.70xVDD	0.78xVDD		V_{SS} = 0 V
$V_{th,2}$	CSD pin self reset threshold	0.26xVDD	0.30xVDD	0.34xVDD		V_{SS} = 0 V
$V_{th,3}$	CT pin shutdown release threshold	0.62xVDD	0.70xVDD	0.78xVDD		V_{SS} = 0 V
I_{CSD+}	CSD pin discharge current	70	100	130	µA	V_{CSD} = V_{SS} +5 V
I_{CSD-}	CSD pin charge current	70	100	130		V_{CSD} = V_{SS} +5 V
I_{CT+}	CT pin charge current	60	95	135		V_{CT} = 5 V
I_{CT-}	CT pin discharge current	6.0	9.5	13.5		V_{CT} = 5 V
t_{SD}	Shutdown propagation delay from V_{CSD} > V_{SS} + V_{thOCH} to Shutdown	—	—	250	ns	
t_{OCH}	Propagation delay time from V_{CSH} >V_{thOCH} to shutdown	—	—	500		
t_{OCL}	Propagation delay time from V_S>V_{thOCL} to shutdown	—	—	500		
t_{OFF}	Fixed gate off time during constant current mode	0.8	1.0	1.2	µS	
t_{PWCT}	Minimum pulse width of CT charging time	—	3	—		

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
Gate Driver						
I_{o+}	Output high short circuit current (Source)	—	1.0	—	A	V_O = 0 V,PW<10 µs
I_{o-}	Output low short circuit current (Sink)	—	1.2	—		V_O=12V,PW<10 µs
V_{OL}	Low level output voltage LO – COM, HO - VS	—	—	0.1	V	
V_{OH}	High level output voltage VCC – LO, VB - HO	—	—	2.0	V	I_O = 0A
t_r	Turn-on rise time	—	15	—	nS	
t_f	Turn-off fall time	—	10	—		
$t_{on,}$	High and low side turn-on propagation delay, floating inputs	—	80	—		$V_{DT} = V_{CC}$, V_S =1 00 V
$t_{off,}$	High and low side turn-off propagation delay, floating inputs	—	65	—		V_{DT}=V_{CC}, V_S = 100 V
D_{T1}	Dead time: LO turn-off to HO turn on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	8	15	22		V_{DT}>V_{DT1}, V_{SS} = COM
D_{T2}	Dead time: LO turn-off to HO turn on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	15	25	35		V_{DT1}>V_{DT}>V_{DT2}, V_{SS} = COM
D_{T3}	Dead time: LO turn-off to HO turn on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	20	35	50		V_{DT2}>V_{DT}>V_{DT3}, V_{SS} =COM
D_{T4}	Dead time: LO turn-off to HO turn on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})V_{DT}= V_{DT4}	25	45	60		V_{DT3}>V_{DT}>V_{DT4}, V_{SS} = COM
V_{DT1}	DT mode select threshold 2	0.51 (V_{CC})	0.57 (V_{CC})	0.63 (V_{CC})	V	
V_{DT2}	DT mode select threshold 3	0.32 (V_{CC})	0.36 (V_{CC})	0.40 (V_{CC})		
V_{DT3}	DT mode select threshold 4	0.21(V_{CC})	0.23 (V_{CC})	0.25 ($_{VCC}$)		

9. TYPICAL APPLICATION CIRCUIT

Note: Please refer to Lead Assignments for correct pin configuration. This diagram shows electrical connections only.

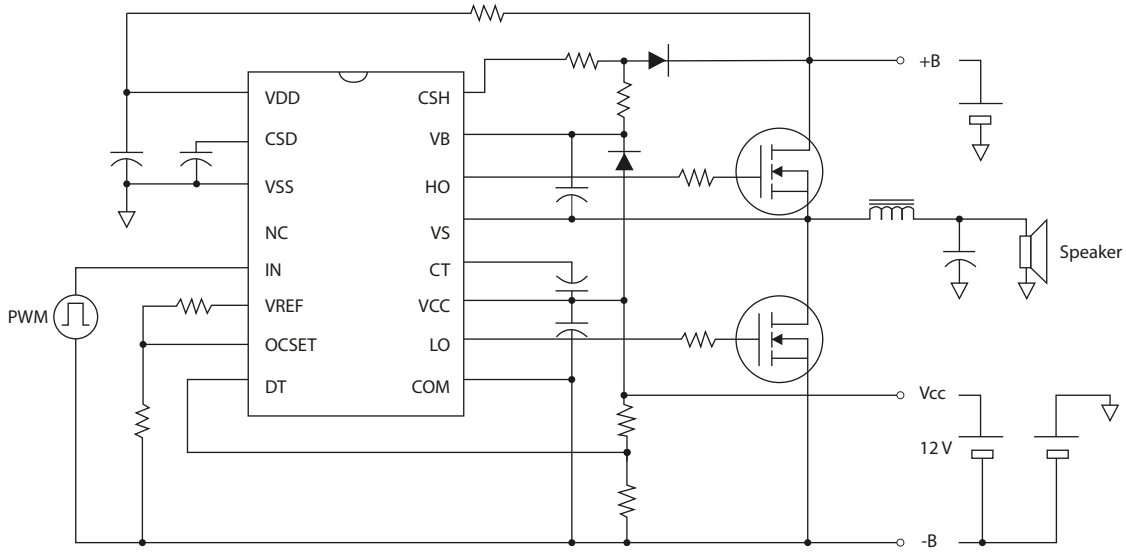

Figure 2. Typical Application Diagram

10. PACKAGE INFORMATION

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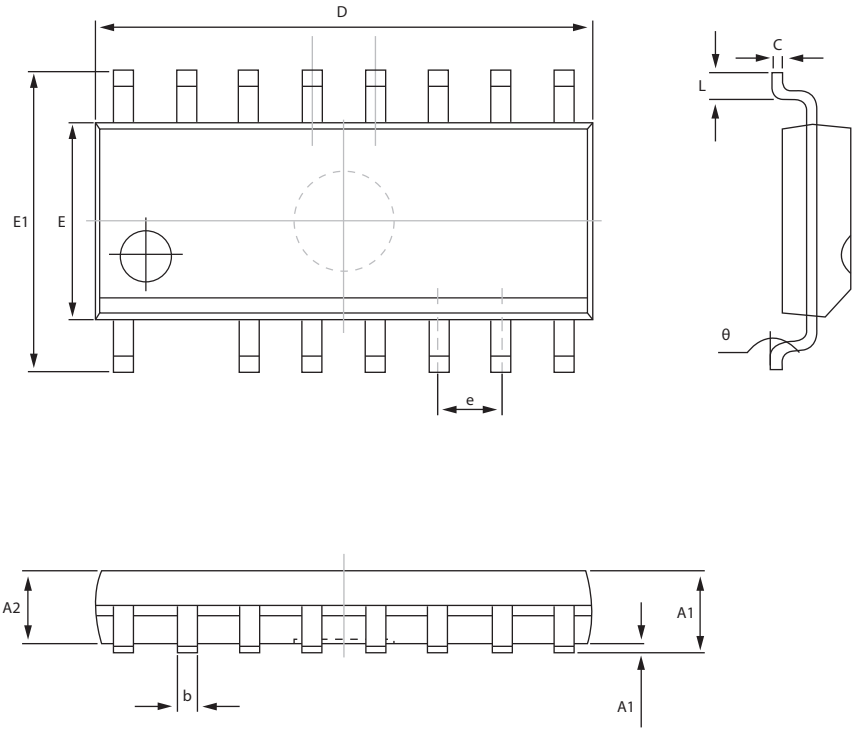

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°